CLASS 712, ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING (E.G. PROCESSORS)

SECTION I - CLASS DEFINITION

This class provides, within a computer or digital data processing system, for subject matter represented by a particular arrangement that includes at least one of the following means: A) components of an individual complete processor, which may be formed on a single integrated circuit (IC); B) components of a complete digital data processing system; C) plural processors; or D) plural digital data processing systems; wherein the particular arrangement further includes at least one of the following functions:

1) processing instruction data for specific processor architectures;

2) accessing or retrieving instruction data of a fixed or variable length from

3) locating and retrieving instruction data for processing;

4) determining via internal hardware, firmware or software operations the

5) dispatching instruction data for execution (e.g., designating a register

6) dynamically testing instruction data and operands to assess conflicts

7) dynamically controlling the execution, processing, or sequencing of

SECTION II - NOTES TO THE CLASS DEFINITION

(1)   Note. Instruction data are defined in the glossary for this class to be data representative of an operation and identifying its operands, if any.

(2)   Note. Process and apparatus for processing instruction data that are classified herein are predicated on a particular, identifiable architecture of a computer or digital data processing system that directs the nature of the processing. Multiple computer and process coordinating (e.g., task management, task control) is classified elsewhere. See SEE OR SEARCH CLASS notes below.

(3)   Note. Register level transactions at the level of the arithmetic logic unit (ALU-level) or functional unit (FU-level) and logic for realizing such transactions are often a part of instruction processing, per se. General purpose, digital logic circuits, however, are classified elsewhere. See SEE OR SEARCH CLASS notes below.

(4)   Note. Exceptions, interrupts, and traps classified herein recite the details of the internal operation of the hardware or the microcode of the processor with only nominal recitation of the stimulus resulting in the exception, interrupt or trap. Process and apparatus for queuing or scheduling interrupts or signals in a computer or digital data processing system are classified elsewhere. See SEE OR SEARCH CLASS notes below. Process and apparatus directed to reliability and testing utilizing halts, interrupts, and traps are also classified elsewhere. See SEE OR SEARCH CLASS notes below.

(5)   Note. Virtual machine or virtual processor is classified elsewhere. See SEE OR SEARCH CLASS notes below.

(6)   Note. Process and apparatus for dynamically aligning instruction data are classified herein. Process and apparatus for shifting memory spaces, such as, boundary alignment related to memory addressing and page mapping are classified elsewhere. See SEE OR SEARCH CLASS notes below. Compilers performing static alignment are classified elsewhere. See SEE OR SEARCH CLASS notes below. Process and apparatus for aligning for data entry or compacting in cache memory typically are classified elsewhere. See SEE OR SEARCH CLASS notes below.

(7)   Note. Emulation for decoding instruction data for execution is classified herein; however, emulation of system component for compatibility is classified elsewhere. See SEE OR SEARCH CLASS notes below.

Emulation directed to testing is also classified elsewhere. See SEE OR SEARCH CLASS notes below.

(8) Note. Process and apparatus for locating and retrieving instruction data in direct support of an instruction pipeline are classified herein; however, process and apparatus for accessing and controlling memory at other higher levels (e.g., cache memory, disk memory, and shared memory) are classified elsewhere. See SEE OR SEARCH CLASS notes below.

(9) Note. Process and apparatus nominally reciting addressing schemes and address data generation may be classified herein; however, process and apparatus for generalized address forming, addressing operands, generating addresses in response to microinstructions, and addressing in combination with particular memory systems are classified elsewhere. See SEE OR SEARCH CLASS notes below.

(10) Note. Process and apparatus for decoding instruction data to determine their meaning for subsequent execution or decision making are classified herein; however, generic decoding circuits, methods, and programs are classified elsewhere. See SEE OR SEARCH CLASS notes below.

(11) Note. Process and apparatus for issuing or dispatching of instruction data to hardware elements internal to a processor for decoding or executing are classified herein; however, process and apparatus for dispatching in the field of process control for task management dealing with process scheduling, load balancing, etc., are classified elsewhere. See SEE OR SEARCH CLASS notes below.

(12) Note. Process and apparatus for dynamically controlling the issuance or execution of instruction data based on analysis of hardware-resource availability, hardware-resource utilization, and data dependency are classified herein; however, processes and apparatus for task resource management are classified elsewhere. See SEE OR SEARCH CLASS notes below. Dependency checking performed by a com-

piler is classified elsewhere. See SEE OR SEARCH CLASS notes below. Process and apparatus for enhancing the reliability and availability of functional units that include determining a fault condition are classified elsewhere. See SEE OR SEARCH CLASS notes below.

(13) Note. Process and apparatus for dealing with resource management problems within a stream of instruction data, generally at the ALU/functional-unit level are classified herein; however, process and apparatus for resource management in a manufacturing environment are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(14) Note. Process and apparatus for reserving the use of functional units at the instruction level of a computer or digital data processing system are classified herein; however, processes and apparatus for reserving seats for travel, entertainment, etc. are classified elsewhere. See SEE OR SEARCH CLASS notes below.

(15) Note. Process and apparatus utilizing hardware or microcode for processing and executing instruction data are classified herein; however, instruction processing being performed by a compiler, by an interpreter, or by an operating system is classified elsewhere. See SEE OR SEARCH CLASS notes below. Process and apparatus for high-level processing of input/output commands are classified elsewhere. See SEE OR SEARCH CLASS notes below. Process and apparatus for the sequencing common in computerized numerical controllers (CNC), industrial controllers, computer driven machining, etc., is classified elsewhere. See SEE OR SEARCH CLASS notes below.

(16) Note. Hardwired sequencers are also often referred to as sequential state machines in the art. They are appropriately classified herein when they are performing control or sequencing of instruction data within a processor.

(17) Note. Process and apparatus for graphic command processing are classified else-

where. See SEE OR SEARCH CLASS notes below.

SECTION III - REFERENCES TO OTHER CLASSES

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, appropriate subclasses for generic digital logic devices, circuitry, and subcombinations thereof, wherein nonarithmetical operations are performed upon discrete electrical signals representing a value normally described by numerical digits, particularly subclasses 37+ for programmable circuits such as Programmable Logic Arrays (PLA) and subclasses 105+ for decoding circuitry.

340, Communications: Electrical, subclasses 825 through 825.98 for controlling one or more devices to obtain a plurality of results by transmission of a designated one of plural distinctive control signals over a smaller number of communication lines or channels, particularly subclasses 2.1-2.8 for path selection, subclasses 3.1-3.9 for communication systems where status of a controlled device is communicated, subclass 825.02 for tree or cascade selective communication, subclasses 825.2-825.21 for synchronizing selective communication systems, subclasses 825.5-825.51 for lockout or priority in selective communication systems, subclasses 825.52 and 825.53 for addressing in selective communication system, and subclasses 825.57-825.69 for pulse responsive actuation in selective communication system.

345, Computer Graphics Processing, Operator Interface Processing, And Selective Visual Display Systems, particularly subclasses 502+ for a computer graphic processor system which includes plural graphics processors, subclass 522 for graphic command processing

370, Multiplex Communications, appropriate subclasses for the simultaneous transmission of two or more signals over a common medium, particularly subclasses 254+ for network configuration determination, subclasses 351+ for path finding or routing including packet switching, circuit switching, ATM switching, and subclasses 465+ for adaptive communication protocol.

377, Electrical Pulse Counters, Pulse Dividers, and Shift Registers: Circuits and Systems, various subclasses for generic circuits for pulse counting.

380, Cryptography, appropriate subclasses for cryptographic apparatus or process in general which includes electric signal modification.

381, Electrical Audio Signal Processing Systems and Devices, various subclasses for wired one-way audio systems, per se.

700, Data Processing: Generic Control Systems or Specific Applications, subclasses 1 through 89 for generic data processing control systems and subclasses 90-306 for specific data processing application.

701, Data Processing: Vehicles, Navigation, and Relative Location, subclasses 1+ for vehicle control, guidance, operation, or indication, subclasses 200+ for navigation, and subclasses 300+ for relative location determination.

702, Data Processing: Measuring, Calibrating or Testing, appropriate subclasses for testing measuring or calibrating, particularly subclass 186 for computer and peripheral benchmarking.

703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.

704, Data Processing: Speech Signal Processing, Linguistics, Language Translation, and Audio Compression/ Decompression, subclasses 1+ for linguistics; subclasses 200+ for speech audio processing, subclasses 500 through 504 for audio signal time or bandwidth compression or expansion.

705, Data Processing: Financial, Business Practice, Management, or Cost/Price Determination, particularly subclasses 5+ for reservation, check-in, and booking for reserving space, subclasses 8+ for scheduling and allocating resources for administrative functions, and subclasses 64 - 79 for a cryptographically protected EFT transaction.

706, Data Processing: Artificial Intelligence, subclasses 1+ for fuzzy logic hardware; subclass 10 for plural processing intelligence systems, subclass 11 for artificial intelligence system having particular user interface; subclasses 12+ for machine learning system, subclass 14 for adaptive system; subclasses 15+ for neural network; and subclasses 45+ for knowledge processing system.

707, Data Processing: Database and File Management or Data Structures, particularly subclasses 1 through 10 for database or file accessing, subclasses 100-104.1 for database scheme or structure, and subclasses 200-206 for file or database management.

708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 1+ for electrical hybrid calculating computer, subclasses 100+ for electrical digital calculating computer, and subclasses 800+ for electrical analog calculating computer.

709, Electrical Computers and Digital Processing Systems: Multiple Computer and Process Coordinating, subclasses 1+ for task management or task control, particularly subclass 7 for dependency checking amongst processes and tasks and subclasses 200+ for transferring data between plural, spatially distributed computers or digital data processing systems.

710, Electrical Computers and Digital Processing Systems: Input/Output, appropriate subclasses for interconnecting or transferring data among processors, memories, and peripherals for of computers or digital data processing systems particularly subclasses 260+ for interrupt processing.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 1+ for addressing in combination with particular memory systems; particularly subclass 2 for addressing extended or expanded memory; subclass 5 for addressing multiple memory modules; subclasses 101+ for accessing and control of specific memory compositions; subclasses 118+ for cache memory; subclasses 147+ for shared memory access and control; subclass 159 for memory entry replacement strategies; subclass 201 for address generation directed to slip control, misalignment, and boundary alignment; subclass 209 for page address generation processing; and subclass 212 for address generation by varying bit-length or size; subclass 214 for operand address generation; and subclass 215 for address formation in response to a microinstruction;

713, Electrical Computers and Digital Processing Systems, subclasses 1+ for computer initialization or configuration, subclasses 100+ for reconfiguration, subclasses 150 - 181 for multiple computer communication protection by cryptography, subclass 187 for computer program modification detection by cryptography, subclass 188 for computer virus detection by cryptography, subclasses 200+ for security, subclasses 300+ for computer power control, and subclasses 400-601 for synchronization or clock control in a digital data processing.

714, Error Detection/Correction and Fault Detection /Recovery, particularly subclass 707 for synchronization control using an error rate; subclass 731 for a reference timing function or a clock pulse generator in a scan path testing system; subclass 744 for clock or synchronization in digital logic testing using a test pattern generator; and subclass 798 for error detection for synchronization control.

715, Data Processing: Presentation Processing of Document, appropriate subclasses for document presentation processing.

716, Data Processing: Design and Analysis of Circuit or Semiconductor Mask, appropriate subclasses.

717, Data Processing: Software Development, Installation, and Management, appropriate subclasses for a software development tool, particularly, subclasses 140 through 161 for compilers and compiler-related dependency checking.

SECTION IV - GLOSSARY

BUS

A conductor used for transferring data, signals, or power.

COMPUTER

A machine that inputs data, processes data, stores data, and outputs data.

DATA

Representation of information in a coded manner suitable for communication, interpretation, or processing.

Address data-Data that represent or identify a source or destination.

Instruction data-Data that represent an operation and identify its operands, if any.

Status data-Data that represent conditions of data, digital data processing systems, computers, peripherals, memory, etc.

User data-Data other than address data, instruction data, or status data.

DATA PROCESSING

See PROCESSING, below.

DIGITAL DATA PROCESSING SYSTEM

An arrangement of processor(s) in combination with either memory or peripherals, or both, performing data processing.

ERROR

Manifestation of a fault as an undesired event that occurs when actual behavior deviates from the behavior that is required by initial specifications.

FAILURE

Manifestation of an error as a nonperformance of an expected system service as required by the initial specifications.

FAULT

A flaw in a functional unit (hardware or software).

INFORMATION

Meaning that a human being assigns to data by means of the conventions applied to that data.

MEMORY

A functional unit to which data can be stored and from which data can be retrieved.

PERIPHERAL

A functional unit that transmits data to or receives data from a computer to which it is coupled.

PROCESSING

Methods or apparatus performing systematic operations upon data or information exemplified by functions such as data or information transferring, merging, sorting, and computing (i.e., arithmetic operations or logical operations).

(1)   Note.In this class, the glossary term data is used to modify processing in the term data processing; whereas the term digital data processing system refers to a machine performing data processing.

(2)   Note.In an effort to avoid redundant constructions, in this class, where appropriate, the term address data processing is used in place of address data data processing.

PROCESSOR

A functional unit that interprets and executes instruction data.

RECOVERY

Responding to a fault in a system by either returning a system to a previous level of correct operation, achieving a degraded level of correct operation, or safely shutting down the system.

SECURITY

Extent of protection for system hardware, software, or data from maliciously caused destruction, unauthorized modification, or unauthorized disclosure.

SUBCLASSES

1   **PROCESSING ARCHITECTURE:**
This subclass is indented under the class definition. Subject matter comprising a particular arrangement of (a) elements of an individual complete processor which may be formed on a single integrated chip, (b) components of a complete digital data processing system, (c) plural processing elements, (d) plural processors, or (e) plural digital data processing systems where processing is performed on a generic instruction or process.

(1)   Note.   This subclass and its indents require more than nominal recitation of the architecture of processing elements or operations.

(2)   Note.   Implementation of a generic instruction within a particular instruction set is classified here.

(3) Note. Architecture based instruction processing including specific instruction implementation, such as, branching, store multiple, etc. are classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
200+, for architecture based instruction processing including specific instruction implementation, such as, branching, store multiple, etc.

SEE OR SEARCH CLASS:
340, Communications: Electrical, subclasses 825 through 825.98 for controlling one or more devices to obtain a plurality of results by transmission of a designated one of plural distinctive control signals over a smaller number of communication lines or channels, particularly subclasses 2.1-2.8 for path selection, subclasses 3.1-3.9 for communication systems where status of a controlled device is communicated, subclass 825.02 for tree or cascade selective communication, subclasses 825.2-825.21 for synchronizing selective communication systems, subclasses 825.5-825.51 for lockout or priority in selective communication systems, subclasses 825.52 and 825.53 for addressing, and subclasses 825.57-825.69 for pulse responsive actuation.
345, Computer Graphics Processing, Operator Interface Processing, And Selective Visual Display Systems, subclasses 502+, for a computer graphic processor system which includes plural graphics processors.
370, Multiplex Communications, for the simultaneous transmission of two or more signals over a common medium where the transmitted data is generic to the transmission activity, particularly subclasses 351+ for time division multiplex (TDM) switching, subclasses 475 for asynchronous TDM communications including addressing, and subclasses 498+ for time division bus transmission.

700, Data Processing: Generic Control Systems or Specific Applications, subclass 249 for plural processor robot control.
708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 100+ and particularly subclasses 200+ for an electric digital calculating computer which may utilize processor structure similar to that contained herein.
709, Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 200+ for data transfer between plural spatially distributed computers or digital data processing systems.
710, Electrical Computers and Digital Processing Systems: Input/Output, subclasses 100+ for particular intrasystem connecting (e.g., bus transaction processing) not included in a particular processing architecture, and subclasses 260+ for general interrupt processing.
717, Data Processing: Software Development, Installation, and Management, subclasses 149 and 150 for program code translating or compiling for multiprocessor system.

2 **Vector processor:**
This subclass is indented under subclass 1. Subject matter including specificadaptation of the architecture or structure which operates on one-dimensional data arrays.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
10+, for array processor architecture, in general.

SEE OR SEARCH CLASS:
708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 100+ and particularly subclasses 200+ for an electric digital calculating computer which may utilize processor structure similar to that contained herein.

3   **Scalar/vector processor interface:**
This subclass is indented under subclass 2. Subject matter which includes an intermediate structure linking a scalar processor with a vector processor.

4   **Distributing of vector data to vector registers:**
This subclass is indented under subclass 2. Subject matter involving structure providing vector data transfer to vector registers.

SEE OR SEARCH CLASS:
709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 200+ for data transfer between plural complete spatially distributed computers or digital data processing systems.

5   **Masking to control an access to data in vector register:**
This subclass is indented under subclass 4. Subject matter which is directed to specific structure or operation to screen out access to a particular location in a vector register.

6   **Controlling access to external vector data:**
This subclass is indented under subclass 2. Subject matter wherein access to external vector processing data is regulated.

7   **Vector processor operation:**
This subclass is indented under subclass 2. Subject matter wherein functioning of the vector processor is specified.

8   **Sequential:**
This subclass is indented under subclass 7. Subject matter wherein a vector processing is performed in program order.

9   **Concurrent:**
This subclass is indented under subclass 7. Subject matter wherein multiple vector instructions are issued simultaneously.

10   **Array processor:**
This subclass is indented under subclass 1. Subject matter comprising four or more identical processing elements (e.g., cells) joined in a two-dimensional or higher arrangement.

SEE OR SEARCH CLASS:
708,   Electrical Computers: Arithmetic Processing and Calculating, subclasses 100+ and particularly subclasses 200+ for an electric digital calculating computer which may utilize processor structure similar to that contained herein.

11   **Array processor element interconnection:**
This subclass is indented under subclass 10. Subject matter including details of a structure which mutually joins the identical processing elements.

SEE OR SEARCH CLASS:
710,   Electrical Computers and Digital Processing Systems-Input/Output, subclasses 100+ for particular intrasystem connecting (e.g., bus transaction processing) not included in a particular array processing architecture.

12   **Cube or hypercube:**
This subclass is indented under subclass 11. Subject matter wherein the identical processing elements are joined in a 3-or - greater dimensional pattern.

13   **Partitioning:**
This subclass is indented under subclass 11. Subject matter which controls the structure joining the processing elements by partitioning the array into groups of processing elements.

SEE OR SEARCH CLASS:
711,   Electrical Computers and Digital Processing Systems: Memory, subclass 129 for partitioned cache accessing and control.

14   **Processing element memory:**
This subclass is indented under subclass 11. Subject matter which controls the structure joining the memory within an individual array processor element or associated with an individual array processor element.

15   **Reconfiguring:**
This subclass is indented under subclass 11. Subject matter wherein an existing structure joining the array processing elements is modified.

SEE OR SEARCH CLASS:

709, Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 221+ for reconfiguring in a multi-computer data transfer network.

710, Electrical Computers and Digital Processing Systems: Input/Output, subclass 104 for intra-system configuring not included in a particular processing architecture.

713, Electrical Computers and Digital Processing Systems: Support, subclass 100 for reconfiguring (e.g., changing system setting) in a digital data processing system.

16   Array processor operation:
This subclass is indented under subclass 10. Subject matter wherein a specific function or process performed by the array processor is specified.

17   Application specific:
This subclass is indented under subclass 16. Subject matter wherein overall operation or process of the array processor is directed toward a particular purpose.

(1)   Note.   Included here, for example, is generic pattern matching not elsewhere provided for.

(2)   Note.   Pattern matching for image processing is classified elsewhere.

SEE OR SEARCH CLASS:

382,   Image Analysis, appropriate subclasses and particularly subclasses 181+ for image analysis pattern recognition.

18   Data flow array processor:
This subclass is indented under subclass 16. Subject matter wherein the array processor performs a calculation when all required data is present (data-driven).

(1)   Note.   This would include a wavefront array processor.

SEE OR SEARCH THIS CLASS, SUBCLASS:

25,   for a generic data flow processor.
201,   for architecture based data flow instruction processing including specific instruction implementation.

19   Systolic array processor:
This subclass is indented under subclass 16. Subject matter wherein data moves between the identical processing elements in accordance with a global reference timing signal.

20   Multimode (e.g., MIMD to SIMD, etc.):
This subclass is indented under subclass 16. Subject matter wherein the array processor may switch between plural operating modes.

(1)   Note.   This might include, for example, an initial MIMD mode which subsequently changes to an SIMD mode.

21   Multiple instruction, multiple data (MIMD):
This subclass is indented under subclass 16. Subject matter wherein the array processor operates in a multiple instruction, multiple data mode.

22   SIMD:
This subclass is indented under subclass 16. Subject matter wherein the array processor operates in a single instruction, multiple data mode.

23   Superscalar:
This subclass is indented under subclass 1. Subject matter comprising an architecture which determines a group of upcoming instructions which do not mutually interfere with each other and issues or dispatches this group simultaneously.

(1)   Note.   Excluded herein is specific instruction implementation such as branching, store multiple, etc. See SEE OR SEARCH THIS CLASS, SUBCLASS: notes below.

(2)   Note.   Implementation of a generic instruction within a particular instruction set is classified here.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
215, for simultaneous issuance of multiple instructions including specific instruction implementation.

24 Long instruction word:
This subclass is indented under subclass 1. Subject matter comprising an architecture which includes compiler scheduled issuing of multiple opcodes per instruction.

(1) Note. Excluded herein is the specifics of the compiler.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
215, for simultaneous issuance of multiple instructions including specific instruction

SEE OR SEARCH CLASS:
717, Data Processing: Software Development, Installation, and Management, subclasses 140 through 161 for a compiler in a software development system.

25 Data driven or demand driven processor:
This subclass is indented under subclass 1. Subject matter wherein a plural processor structure performs a calculation when all required data is present (data-driven) or when other processors request a calculation result (demand-driven).

SEE OR SEARCH THIS CLASS, SUB-CLASS:
18, for data flow array processor.
201, for architecture based data flow instruction processing including specific instruction implementation.

26 Detection/pairing based on destination, ID tag, or data:
This subclass is indented under subclass 25. Subject matter which is directed to specific structure or operation to perform detecting or pairing dependent upon intended destination, a particular identification tag or data itself.

27 Particular data driven memory structure:
This subclass is indented under subclass 25. Subject matter including a data driven interface with specific memory structure to enhance the data flow capability of the processor.

SEE OR SEARCH CLASS:
711, Electrical Computers and Digital Processing Systems: Memory, subclasses 100+ for particular storage accessing and control.

28 Distributed processing system:
This subclass is indented under subclass 1. Subject matter including a particular architecture having two or more physically separate processors performing different tasks with shared resources such that their combined work contribute to a common goal.

(1) Note. Subject matter including a distributed processing system having significant multicomputer data transfer is classified elsewhere. See SEE OR SEARCH CLASS below.

(2) Note. Subject matter including a computer task management or control system having significant process scheduling is classified elsewhere. See SEE OR SEARCH CLASS below.

SEE OR SEARCH CLASS:
709, Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 3+ for process scheduling in a computer task management or control system, subclass 201 for distributed data processing having significant multicomputer data transfer.

29 Interface:
This subclass is indented under subclass 28. Subject matter wherein details of an interconnection which mutually joins the processors are provided.

30 Operation:
This subclass is indented under subclass 28. Subject matter wherein functioning of the processors is specified.

**31	Master/slave:**
This subclass is indented under subclass 30. Subject matter wherein the physically separate processors include a primary processor (master) controlling the operation of a secondary processor (slave).

(1)	Note.	Controlling of data transfer between master/slave processors is classified elsewhere.

SEE OR SEARCH CLASS:
345,	Computer Graphic Processing, Operator Interface Processing, and Selective Visual Display Systems, subclass 504 for a computer graphic processing system including master/slave processors.
709,	Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 208+ for specific data transferring in a master/slave computer.
710,	Electrical Computers and Digital Processing Systems-Input/Output, subclass 110 for bus master/slave controlling.

**32	Microprocessor or multichip or multimodule processor having sequential program control:**
This subclass is indented under subclass 1. Subject matter comprising a CPU on a single integrated circuit chip or on plural integrated chips or in plural discrete units which provide serial processing.

SEE OR SEARCH CLASS:
345,	Computer Graphic Processing, Operator Interface Processing, and Selective Visual Display Systems, subclass 519 for a computer graphic processing system on integrated chip.
708,	Electrical Computers: Arithmetic Processing and Calculating, subclasses 100+ and particularly subclasses 200+ for an electric digital calculating computer which may utilize processor structure similar to that contained herein.

**33	Having multiple internal buses:**
This subclass is indented under subclass 32. Subject matter comprising an internal structure having plural buses.

**34	Including coprocessor:**
This subclass is indented under subclass 32. Subject matter including an auxiliary processor which provides a supplemental function for or other assistance to a primary processor.

(1)	Note.	Details of the application or algorithm performed on the coprocessor are classified elsewhere. See, for example, SEE OR SEARCH CLASS below.

SEE OR SEARCH CLASS:
345,	Computer Graphic Processing, Operator Interface Processing, and Selective Visual Display Systems, subclass 503 for a computer graphic processing system which includes a coprocessor.

**35	Digital Signal Processor:**
This subclass is indented under subclass 34. Subject matter wherein the auxiliary processor is particularly configured to perform high speed data manipulations.

(1)	Note.	Details of the application or algorithm performed on the Digital Signal Processor are classified elsewhere. See, for example, SEE OR SEARCH CLASS below.

SEE OR SEARCH CLASS:
708,	Electrical Computers: Arithmetic Processing and Calculating, subclasses 100+ for an electric digital calculating computer.

**36	Application specific:**
This subclass is indented under subclass 32. Subject matter wherein the processor is generically adapted for a particular purpose.

(1)	Note.	Details of the application or algorithm performed on the processor are classified elsewhere.

37   Programmable (e.g., EPROM):
This subclass is indented under subclass 32. Subject matter wherein operation of the processor may be externally modifiable.

SEE OR SEARCH CLASS:
713,   Electrical Computers and Digital Processing Systems: Support, subclasses 1+ for digital data processing system initialization and configuration.

38   Offchip interface:
This subclass is indented under subclass 32. Subject matter wherein particular internal structure of the processor is provided which allows interfacing from the processor to an external device.

SEE OR SEARCH CLASS:
710,   Electrical Computers and Digital Data Processing Systems: Input/Output, subclass 1 for input/output data processing and subclasses 305-317 for interface architecture intra-system connection.

39   Externally controlled internal mode switching via pin:
This subclass is indented under subclass 38. Subject matter wherein an internal processor mode may be changed by an external means connected to the processor by an electrical contact.

40   External sync or interrupt signal:
This subclass is indented under subclass 38. Subject matter wherein the processor receives a synchronization or interrupt signal from an outside source.

SEE OR SEARCH CLASS:
709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclass 400 synchronization of plural processors.
710,   Electrical Computers and Digital Processing Systems: Input/Output, subclasses 260+ for interrupt processing in general.

41   RISC:
This subclass is indented under subclass 32. Subject matter wherein the set of processing instructions available is relatively small and rapidly executable (i.e., Reduced Instruction Set Computing) and a new instruction is fetched during the time when a previous instruction is executed.

42   Operation:
This subclass is indented under subclass 32. Subject matter wherein specific functioning of the processor is recited.

43   Mode switching:
This subclass is indented under subclass 42. Subject matter wherein an ability to change between multiple processor operating modes is recited.

200   ARCHITECTURE BASED INSTRUCTION PROCESSING:
This subclass is indented under the class definition. Subject matter including instruction data processing for particular processor architectures.

(1)   Note. Instruction data are defined in the glossary for this class to be data representative of an operation and identifying its operands, if any.

(2)   Note. Instruction processing classified here is predicated on a particular identifiable digital data processing system architecture directing the nature of the instruction processing. Processing control, however, is classified elsewhere. See SEARCH THIS CLASS,SUBCLASS below.

(3)   Note. This subclass is for instruction processing forced in a certain direction by an overall processing architecture. Digital data processing system architectures and computer architectures, per se, are classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS: below.

(4)   Note. Register level transactions at the arithmetic logic unit level (ALU-level) or functional unit level (FU-level) and

logic for realizing such transactions are often a part of instruction processing, per se. However, general purpose digital logic circuits are classified elsewhere. See SEE OR SEARCH CLASS below.

(5)   Note. This subclass represents a "special" category of instruction processing dictated by an architectural construct. Instruction data processing in support of data transferring including special software interrupts, traps, and halts; non-logic and non-arithmetic functions are classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS: below.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
1+,   for digital data processing system architectures and computer architectures per se.
25,   for instruction data processing in support of data transferring.
220+,   for processing control, per se.
227,   for special instruction data processing in support of testing, debugging, or emulation.
244,   for software interrupts and traps.

SEE OR SEARCH CLASS:
326,   Electronic Digital Logic Circuitry, appropriate subclasses for general purpose digital logic circuitry including programmable logic arrays (PLA).
708,   Electrical Computers: Arithmetic Processing and Calculating, subclasses 100+ for details of logic circuits for performing arithmetic operations.
714,   Error Detection/Correction and Fault Detection/Recovery, subclass 34 for fault locating using a halt, subclass 35 for fault locating using a substituted or added instruction.
717,   Data Processing: Software Development, Installation, and Management, subclasses 100 through 173 for software development environments and tools, per se.

201   Data flow based system:
This subclass is indented under subclass 200. Subject matter wherein initiation of instruction execution is driven by availability of data required by the instruction.

(1)   Note. This subclass is for data flow computing which generally utilizes tokens for asynchronous passing of instructions or data for execution by the appropriate unit.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
18,   for data flow array processor.
25,   for data flow computer architectures, per se.

SEE OR SEARCH CLASS:
709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 200+ for use of tokens in certain multi-computer arrangements.

202   Stack based computer:
This subclass is indented under subclass 200. Subject matter wherein the architecture's processor is based upon a stack model and all instruction data processing occurs through use of the stack.

(1)   Note. The stack based computer includes, for example, HP 3000 computer.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
228,   for context preservation.

SEE OR SEARCH CLASS:
709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, for pertinent subclass(es) as determined by schedule review.

203   Multiprocessor instruction:
This subclass is indented under subclass 200. Subject matter including processing of an instruction specific for a plural processor computer architecture.

SEE OR SEARCH THIS CLASS, SUB-CLASS:

28+,   for a distributed processing system.

32+,   for microprocessor or multichip or multimodule processor having sequential

204   **INSTRUCTION ALIGNMENT:**

This subclass is indented under the class definition. Subject matter including accessing and retrieval of instruction data of a fixed or variable length from a memory or buffer and for shifting of such instruction data to align it with a physical memory or buffer boundary.

(1)   Note. This subclass is for alignment of instruction data. Subject matter directed to the big endian/ little endian problem is properly classified here. Generic byte word order rearranging is classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS below.

(2)   Note. This subclass accepts shifting instruction data for alignment purposes. Shifting of memory spaces, such as boundary alignment related to memory addressing and page mapping, is classified elsewhere. See SEE OR SEARCH CLASS below.

(3)   Note. Emulation techniques often rely on instruction alignment as part of an overall combination. This subclass accepts only nominal recitations to emulation in combination with instruction aligning. Emulation systems, per se, are classified elsewhere. See SEE OR SEARCH CLASS below.

(4)   Note. This subclass accepts only nominal recitations to digital data processing system architectures and computer architectures, per se, where realignment of an instruction is occurring. Architecture-based instruction data processing in, for example, a superscalar processor is classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS below.

(5)   Note. Dynamic aligning of instruction data is proper for this subclass. Compil-

ers performing "static" alignment functions are classified with software development tools. See SEE OR SEARCH CLASS below.

(6)   Note. This subclass is directed to aligning instruction data. Aligning other data in, for example, cache memory is typically found elsewhere. See SEE OR SEARCH CLASS below.

SEE OR SEARCH THIS CLASS, SUB-CLASS:

23,   for superscalar processor.

200+,   for architecture based instruction data processing.

210,   for variable length instruction data decoding.

300,   for generic byte-word order rearranging, bit-field insertion and extraction, and string length and sequence detecting.

SEE OR SEARCH CLASS:

703,   Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.

711,   Electrical Computers and Digital Processing Systems: Memory, subclass 2 for addressing extended or expanded memory, subclass 5 for addressing multiple memory modules, subclass 118 for cache memory accessing and control, per se, subclass 133 for cache memory entry replacement strategies, subclass 201 for address generation directed to slip control, misaligning and boundary alignment, subclass 209 for page address generation processing, subclass 212 for address generation by varying bit-length or size.

716,   Data Processing: Design and Analysis of Circuit or Semiconductor Mask, appropriate subclasses.

717,   Data Processing: Software Development, Installation, and Management, subclasses 140 through 161 for compilers, per se.

205   **INSTRUCTION FETCHING:**

This subclass is indented under the class definition. Subject matter directed to locating and retrieval of instruction data for processing.

(1) Note. This subclass is concerned with locating and retrieving instruction data indirect support of an instruction pipeline. Memory accessing and control at other higher levels, such as, cache memory, disk memory and shared memory are classified elsewhere. See SEE OR SEARCH CLASS below.

(2) Note. This subclass only accepts nominal recitation of addressing schemes and address data generation. Address formation, addressing of operands, and address generation in response to a microinstruction is elsewhere. See SEE OR SEARCH CLASS below.

(3) Note. This subclass only accepts nominal recitation of addressing schemes and address data generation. Generalized address formation and addressing in combination with particular memory systems is classified elsewhere. See SEE OR SEARCH CLASS below.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Processing Systems: Input/Output, subclasses 5+ for Input/Output data processing macro language and command processing
711, Electrical Computers and Digital Processing Systems: Memory, subclasses 1+ for addressing combined with specific memory configuration or system, subclasses 101+ for accessing and control of specific memory compositions, subclasses 118+ for cache memory, and subclasses 147+ for shared memory access and control, subclass 214 for operand address generation, and subclass 215 for address formation in response to a microinstruction.

206 Of multiple instructions simultaneously:
This subclass is indented under subclass 205. Subject matter for causing a fetch of a plurality of instruction data to occur at the same time.

207 Prefetching:
This subclass is indented under subclass 205. Subject matter including fetching of a given instruction or variable before it is utilized.

(1) Note. This subclass provides for advance fetching of instruction data. pipelining is classified elsewhere. Memory access

(2) Note. This subclass is for the fetching of instruction data. Generating of addresses for implementing a prefetch is classified elsewhere.

(3) Note. Prefetching for branch target addressing is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
237, for branch target instruction addressing.

SEE OR SEARCH CLASS:
711, Electrical Computers and Digital Processing Systems: Memory, subclass 169 for memory access pipelining, and subclass 213 for formation or generation of prefetch addresses.

208 INSTRUCTION DECODING (E.G., BY MICROINSTRUCTION, START ADDRESS GENERATOR, HARDWIRED):
This subclass is indented under the class definition. Subject matter including an internal hardware, firmware, or software operation by which a computer system determines the meaning of an instruction's operation code, control bits, and operands.

(1) Note. This subclass is for decoding instruction data to determine its meaning for subsequent execution or decision making. Generic decoding circuits and methods and decoder circuits and methods are classified elsewhere. See SEE OR SEARCH CLASS below.

SEE OR SEARCH CLASS:
326, Electronic Digital Logic Circuitry, subclasses 105+ for decoding circuitry.

209   **Decoding instruction to accommodate plural instruction interpretations (e.g., different dialects, languages, emulation, etc.):**
This subclass is indented under subclass 208. Subject matter including means or steps for decoding a same instruction identifier to mean a different operation depending on a particular state or condition within the system.

(1)   Note. This subclass is for instruction decoding for plural interpretations. Emulation, per se, is classified elsewhere. See SEE OR SEARCH CLASS note below.

SEE OR SEARCH CLASS:
703,   Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.
704,   Data Processing: Speech Signal Processing, Linguistics, Language Translation, and Audio Compression/ Decompression, subclasses 2+ for translation machine, subclass 9 for natural language translation.
716,   Data Processing: Design and Analysis of Circuit or Semiconductor Mask, appropriate subclasses.
717,   Data Processing: Software Development, Installation, and Management, subclasses 140 through 161 for compilers, per se.

210   **Decoding instruction to accommodate variable length instruction or operand:**
This subclass is indented under subclass 208. Subject matter including means or steps for decoding instruction data whose length varies.

(1)   Note. This subclass is for decoding instructions whose lengths vary. Alignment of instructions to a boundary is classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS note below.

SEE OR SEARCH THIS CLASS, SUBCLASS:
204,   for alignment of instruction data.

211   **Decoding instruction to generate an address of a microroutine:**
This subclass is indented under subclass 208. Subject matter including means or steps for utilizing instruction data to develop a starting or initial address of a microroutine responsible for controlling execution of the instruction.

SEE OR SEARCH CLASS:
711,   Electrical Computers and Digital Processing Systems: Memory, subclass 215 for generation of a memory address in response to a microroutine.

212   **Decoding by plural parallel decoders:**
This subclass is indented under subclass 208. Subject matter including means or steps for decoding an instruction in parallel steps by plural decoding elements.

SEE OR SEARCH THIS CLASS, SUBCLASS:
1+,   for parallel computer architecture.

213   **Predecoding of instruction component:**
This subclass is indented under subclass 208. Subject matter for decoding part of an instruction at an earlier processor cycle than the remainder of the instruction.

(1)   Note. This subclass will accept only nominal recitations of instruction caching in regards to pre-decoding. Caching, per se, is classified elsewhere.

(2)   Note. This technique is often used in combination with branch instruction processing in order to prefetch for anticipated branch execution and in parallel processing. This subclass accepts only significant recitations of pre-decoding in overall combinations directed to prefetching, branch instruction processing, and parallel processing. Prefetching, branch instruction processing, and parallel processing, per se, are classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS: below.

SEE OR SEARCH THIS CLASS, SUBCLASS:
207,   for instruction prefetching.

215, for decoding for data dependency processing for parallel issuance.
233+, for branching.

214 INSTRUCTION ISSUING:
This subclass is indented under the class definition. Subject matter including means or steps for dispatching an instruction for execution (e.g., designating a register after resolving data conflicts).

(1) Note. Dispatching in the field of process control for task management dealing with process scheduling, load balancing, etc., is classified elsewhere. See SEE OR SEARCH CLASS below.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
201, for data flow architecture based instruction processing system.

SEE OR SEARCH CLASS:
709, Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 1+ for task management or task control.

215 Simultaneous issuance of multiple instructions:
This subclass is indented under subclass 214. Subject matter including means or steps for issuing plural instructions in parallel (e.g., superscalar, very long instruction word (VLIW)).

(1) Note. This subclass provides for dynamic, hardware-based multiple instruction issuance or scheduling. Static instruction scheduling by a compiler or an assembler is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
23, for superscalar processing architecture.
24, for long instruction word processing architecture.

SEE OR SEARCH CLASS:
717, Data Processing: Software Development, Installation, and Management, subclasses 140 through 161 for compilers, per se.

216 DYNAMIC INSTRUCTION DEPENDENCY CHECKING, MONITORING, OR CONFLICT RESOLUTION:
This subclass is indented under the class definition. Subject matter including means or steps for on-the-fly testing of instructions and operands to assess conflicts related to data or functional unit availability (e.g., identifying dependencies, attempting to resolve dependencies, or both).

(1) Note. This subclass is directed to means and steps for controlling instruction issuing or executing which takes into account readiness of the instruction processing resource(s). Task resource management is classified elsewhere.

(2) Note. This subclass is also for dynamic hardware based dependency checking. Dependency checking performed by a compiler is classified elsewhere.

(3) Note. Reliability and availability of functional units include the determination of a fault condition and are classified elsewhere.

(4) Note. This subclass includes dealing with resource management problems within the instruction stream, generally at the ALU functional unit level. Resource management in a manufacturing environment is classified elsewhere.

(5) Note. This subclass deals with reserving use of functional units at the instruction level of a digital data processing system. Reservations for seat assignment for travel or entertainment are classified elsewhere.

SEE OR SEARCH CLASS:

700,   Data Processing: Generic Control Systems or Specific Applications, subclasses 99 through 102 for manufacturing environment resource allocation.

705,   Data Processing: Financial, Business Practice Management, or Cost /Price Determination, subclasses 5+ for reservation, check-in, booking for reserving space, and subclass 8+ for scheduling and allocating resources for administrative function in a business environment.

709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclass 7 dependency checking amongst processes and tasks.

711,   Electrical Computers and Digital Processing Systems: Memory, subclass 125 for instruction data caching and subclass 169 for memory access pipelining.

714,   Error Detection/Correction and Fault Detection/Recovery, subclasses 1+ for reliability and availability.

717,   Data Processing: Software Development, Installation, and Management, subclasses 140 through 161 for compilers, per se, and dependency checking.

217   Scoreboarding, reservation station, or aliasing:

This subclass is indented under subclass 216. Subject matter utilizing scoreboarding, reservation stations, aliasing (i.e., renaming), or combinations thereof for dependency checking and resolution.

(1)   Note. This subclass is for use of a hardware-based scoreboard, reservation station, or alias table for determining or resolving instruction data dependencies. File maintenance (e.g., renaming) is classified elsewhere. Task management, per se, is classified elsewhere.

SEE OR SEARCH CLASS:

709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 1+ for task management per se.

707,   Data Processing: Database and File Management, Data Structures, or Document Processing, subclasses 200+ for file renaming or file maintenance.

218   Commitment control or register bypass:

This subclass is indented under subclass 216. Subject matter including means or steps for controlling the writing of results to registers and for bypassing results around registers to eliminate or alleviate data availability conflicts.

(1)   Note. This subclass provides for systems that control the commitment of results to the register file and for bypassing results around the register file to functional units to alleviate data dependency, for example, as in getting data to a functional unit in deeply pipelined or superscalar systems. Data consistency in a cache or cache by-pass is classified elsewhere.

(2)   Note. This subclass provides for out-of - order execution but assures in order commitment of results to the register file. However, memory accessing techniques, per se, are classified elsewhere. See SEE OR SEARCH CLASS note below.

(3)   Note. Context preserving, per se, is classified elsewhere. See SEARCH THIS CLASS, SUBCLASS note below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

228,   for context preservation.

SEE OR SEARCH CLASS:

711,   Electrical Computers and Digital Processing Systems: Memory, subclass 3 for addressing cache memory; subclass 203 for virtual addressing 141+ for cache coherency, in particular subclass 142 for write through and 143

for write back; and subclass 155 for read-modify-write technique.

219   Reducing an impact of a stall or pipeline bubble:
This subclass is indented under subclass 216. Subject matter including means or steps for allowing an instruction execution to catch up with other instruction in a pipeline without flushing that execution pipeline.

(1)   Note. This subclass is directed to reducing a time penalty of pipeline stalls or pipeline bubbles due to data hazards or instruction hazards. Conditional branching creates similar data hazards and pipeline stalls. How ever, pipeline stall or pipeline bubble due to branching are classified elsewhere. See   SEE OR SEARCH THIS CLASS, SUBCLASS note below.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
233+,   for branching when an instruction hazard exists.

SEE OR SEARCH CLASS:
711,   Electrical Computers and Digital Processing Systems: Memory, subclass 140 for data hazards related caching and subclass 169 for memory access pipelining.

220   PROCESSING CONTROL:
This subclass is indented under the class definition. Subject matter including a dynamic control of execution, processing, or sequencing of instruction data within a processor.

(1)   Note. This subclass provides for generic micro-sequencing control or hardware sequencing control of instruction data within a processor.   Specialized architecture-based instruction processing is classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS note below.

(2)   Note.   This subclass is directed to instruction processing and machine level Instruction execution. However, instruction sequence control within a compiler, by a compiler, or by an operating system

is classified elsewhere. See SEE OR SEARCH CLASS note below.

(3)   Note. This subclass is for processing instructions. Sequencing as is common in computerized numerical controllers (CNC), industrial controllers, computer driven machining, etc., is classified elsewhere. See SEE OR SEARCH CLASS note below.

(4)   Note.   Hardwired sequencers are also often referred to as "sequential state machines" in the art. They are appropriately classified here when they are performing control or sequencing of instruction data within a processor.

(5)   Note. Graphic command processing is classified elsewhere. See SEE OR SEARCH CLASS note below.

SEE OR SEARCH THIS CLASS, SUB-CLASS:
200+,   for architecture-based instruction processing.

SEE OR SEARCH CLASS:
345,   Computer Graphic Processing, Operator Interface Processing, and Selective Visual Display Systems, subclass 522 for graphic command processing.
700,   Data Processing: Generic Control Systems or Specific Applications, subclasses 1 through 89 for general purpose computer control systems; subclasses 95-212 for manufacturing control systems; and particularly subclasses 159-195 for machine tool control systems.
709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 1+ operating system task management and control.
717,   Data Processing: Software Development, Installation, and Management, subclasses 140 through 161   for a compiler in a software development system.

221   Arithmetic operation instruction processing:
This subclass is indented under subclass 220. Subject matter for control of execution or processing of instruction data peculiar to arithmetic operation (e.g., add, subtract, multiply, etc.).

(1)   Note. This subclass is directed to control of execution or processing of an instruction peculiar to arithmetic operation. Arithmetic functional units, that is, machines which carry out arithmetical calculations, per se, are classified elsewhere. See SEE OR SEARCH CLASS below.

SEE OR SEARCH CLASS:
708,   Electrical Computers: Arithmetic Processing And Calculating, subclasses 100+ for electrical calculators; subclasses 200+ for specialized functions performed by an electrical digital calculating computer such as function generation and filtering; subclasses 400+ for transforms (e.g., Fourier); subclasses 440+ for trigonometric functions; and subclasses 490+ for arithmetic operations, per se.

222   Floating point or vector:
This subclass is indented under subclass 221. Subject matter for control of execution or processing of instruction data peculiar to a floating point or vector operation.

SEE OR SEARCH CLASS:
708,   Electrical Computers: Arithmetic Processing And Calculating, subclasses 495+ for floating point arithmetical operations.

223   Logic operation instruction processing:
This subclass is indented under subclass 220. Subject matter for control of execution or processing of instruction data peculiar to logic operation (e.g., AND, OR, exclusive OR, etc.).

(1)   Note. This subclass provides for the control of execution of instruction data peculiar to logical operations. Digital logic, per se, (e.g., AND gates, OR gates, combinations of gates, etc.) is classified elsewhere. See SEE OR SEARCH CLASS note below.

(2)   Note. This subclass is concerned with processing instruction data within a processor. Processing of pixels using logical operation in the field of computer graphics processing, however, are classified elsewhere. See SEE OR SEARCH CLASS note below.

SEE OR SEARCH CLASS:
326,   Electronic Digital Logic Circuitry, appropriate subclasses for logic circuit and interface, per se.
345,   Computer Graphic Processing, Operator Interface Processing, and Selective Visual Display Systems, subclasses 523+ for logical operations in computer graphics.

224   Masking:
This subclass is indented under subclass 223. Subject matter for control of execution or processing of instruction data peculiar to blocking and passing data elements contained within memory words or processor registers.

(1)   Note. This subclass provides for control of execution of instruction data which is peculiar to masking. Generic masking of digital words in a digital data processing system is classified elsewhere.

(2)   Note. Masking is a generic technique for stripping, passing, eliminating, or blocking a part of a digital word. Masking used as a subcombination to an overall combination such as, for example, to enable or disable interrupts or to enable or disable a status line is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
5,   for masking to control an access to data in vector register of a vector processor.
300,   for generic masking of digital data.

SEE OR SEARCH CLASS:

710,　Electrical Computers and Digital Processing Systems: Input/Output, subclasses 262+ for interrupt processing in relation to masking.

714,　Error Detection/Correction and Fault Detection/Recovery, subclasses 3+ for masking in relation to fault recovery.

225　Processing control for data transfer:
This subclass is indented under subclass 220. Subject matter including means or steps for processing instruction data that specifically support or perform a data transfer operation.

(1)　Note. This subclass provides for processing instruction data that performs data transfer. Data transfer, per se, is classified elsewhere.

SEE OR SEARCH CLASS:

370,　Multiplex Communications, appropriate subclasses for multiplex communications, per se.

375,　Pulse or Digital Communications, appropriate subclasses for pulse or digital communications, per se.

709,　Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 200+ for multicomputer data transferring .

710,　Electrical Computers and Digital Processing Systems: Input/Output, subclasses 5+ for I/O command processing, subclass 33 for I/O data transfer specifying.

711,　Electrical Computers and Digital Processing Systems: Memory, subclass 214 for operand address generation and subclass 215 for microinstruction address generation.

226　Instruction modification based on condition:
This subclass is indented under subclass 220. Subject matter including means or steps for changing the operation of an instruction based upon some condition by substituting or changing the instruction in some manner.

(1)　Note. This subclass also provides for modification of microinstruction in order to perform a different operation.

(2)　Note. This subclass provides for modification of an instruction to change its operation or data usage. Modification of instruction address for the purpose of branching is classified elsewhere.

(3)　Note. Instruction substitution or modification in support of tracing or fault locating is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
233+,　for branching, per se.

SEE OR SEARCH CLASS:

714,　Error Detection/Correction and Fault Detection/Recovery, subclass 34　for instruction substitution in support of fault locating.

717,　Data Processing: Software Development, Installation, and Management, subclasses 100 through 167　for software development tools.

227　Specialized instruction processing in support of testing, debugging, emulation:
This subclass is indented under subclass 220. Subject matter including means or steps for execution or sequencing of instruction data that support testing, debugging, or emulation.

(1)　Note. Classification in this subclass requires more than nominal recitation of execution of an instruction. Specific means or steps involved in the specific execution of the instruction itself are properly classified in this subclass.

(2)　Note. This subclass is directed to instruction level processing for debugging. A software development environment for compilers is classified elsewhere.

(3)　Note. This subclass is distinguished from the related topics under data processing system reliability and availability. There, a fault condition must be encountered and the fault is either

detected, located, or recovered from, and nominal instruction data processing may be claimed. For classification here, a fault may be nominally recited but substantial instruction processing must be claimed.

(4)   Note. This subclass is distinguished from emulation, per se. There, nominal instruction data processing may be claimed. For classification here, an emulation may be nominally recited, but substantial instruction processing must be claimed.

SEE OR SEARCH CLASS:
703,   Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.
709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 1+ for task management, per se.
714,   Error Detection/Correction and Fault Detection/Recovery, appropriate subclasses, particularly subclasses 35+ for debugging and fault locating.
716,   Data Processing: Design and Analysis of Circuit or Semiconductor Mask, appropriate subclasses.
717,   Data Processing: Software Development, Installation, and Management, subclasses 124 through 135 for software testing or debugging and subclasses 140-161 for compilers, per se.

228   **Context preserving (e.g., context swapping, check-pointing, register windowing):**
This subclass is indented under subclass 220. Subject matter including means for storing volatile data contained in processor registers such that the volatile data can be restored at some point later in time.

(1)   Note. This subclass is directed to the register level transactions necessary for preserving the context of an instruction or an instruction pipeline. Multitasking, context switching, and context swapping at the task or operating system level are classified elsewhere.

(2)   Note. This subclass concerns itself with data in the pipeline at a point in time

when a context swap is to be performed. The control of the commitment of results to a register file or for bypassing results around a register file to functional units to alleviate data dependency is classified elsewhere.

(3)   Note. Transactions with higher level memory in a digital data processing system memory hierarchy such as page swapping or write-back is classified elsewhere with the memory accessing and controlling art.

(4)   Note. The term "windowing" also applies to operator interfaces and often includes logical operations at the register level. However, register windowing here is for instruction registers and instruction pipelines. Windowing for operator interfaces is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
218,   for commitment control or register bypass.

SEE OR SEARCH CLASS:
345,   Computer Graphics Processing, Operator Interface Processing, and Selective Visual Display Systems, subclasses 581-618 for display attribute controller, and subclasses 781 through 807 for operator interface windowing.
709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclass 9 for context switching at the task or operating system level.
711,   Electrical Computers and Digital Processing Systems: Memory, subclass 3 for addressing cache memory; subclasses 141+ for cache coherency, specifically subclass 142 for cache write-through, subclass 143 for cache write-back, and subclasses 203+ for virtual addressing techniques.

229   **Mode switch or change:**
This subclass is indented under subclass 220. Subject matter including means or steps for changing a mode of processing an instruction

(e.g., sequential processing to parallel processing, etc.).

(1)   Note. A digital data processing system can have a variety of mode changes. In general, substantial recitation of a mode change type in combination with nominal recitation of instruction processing is classified with the mode change type. More than nominal recitation of instruction data execution is required for classification herein.

SEE OR SEARCH CLASS:
709,   Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclass 9 for context switching at the task or operating system level.
713,   Electrical Computers and Digital Processing Systems: Support, subclass 2 and 100 for mode changing by booting or reconfiguring, and subclass 200+ for security mode changes.
380,   Cryptography, appropriate subclasses for security, per se.

230   Generating next microinstruction address:
This subclass is indented under subclass 220. Subject matter including means or steps for generating an address of a next microinstruction in sequence to be processed.

(1)   Note. This subclass provides for details of generating a next microinstruction address. Generation of a next microinstruction address is classified elsewhere. Similarly, generation of a next address for a data element, per se, is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
207,   for prefetch of instruction data.
233+,   for branching.

SEE OR SEARCH CLASS:
711,   Electrical Computers and Digital Processing Systems: Memory, subclasses 200+ for address formation.

231   Detecting end or completion of microprogram:
This subclass is indented under subclass 220. Subject matter including means or steps for detecting or sensing a completion or end of a microprogram routine.

(1)   Note. This subclass provides for detection of the completion of execution of a microprogram routine. Macroprogram branching and microprogram branching are classified elsewhere.

(2)   Note. Interruption of the end of a microprogram routine is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
233+,   for macroprogram branching and microprogram branching.
244,   for exception processing or interrupt processing.

232   Hardwired controller:
This subclass is indented under subclass 220. Subject matter utilizing a sequential state machine, hardwired logic, or both for sequencing a flow of instruction data.

(1)   Note. Controlling and sequencing are common functions of digital data processing systems. This subclass provides for details of a processor's internal operation and sequencing of instruction data. Numerical controllers and sequencers, per se, are common in industrial control and are classified elsewhere.

(2)   Note. Hardwired controllers and sequencers are commonly used for their inherent speed advantage. This subclass provides for details of a processor's internal operation and sequencing of instruction data. Hardwired controllers directed to application specific data processing or ASICs (application specific integrated circuits) for specific application, per se, such as digital filtering, graphics data processing, and arithmetic data processing, are classified with the application art area.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclasses 37+ for multifunctional circuits including finite state machines.

345, Computer Graphics Processing, Operator Interface Processing, and Selective Visual Display Systems, subclass 522 for graphic command processing,

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, subclasses 27+ for circuit or device that includes more than a counter or register but is not sufficient for classification with a particular art device; and subclasses 118+ for pulse counting or dividing chains.

700, Data Processing: Generic Control Systems or Specific Applications, subclasses 1 through 89 for industrial controllers and numerical controllers, and subclasses 95-212 for continuous material processing and machine tool control.

703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.

708, Electrical Computers: Arithmetic Processing And Calculating, subclasses 200+ for specialized function performed, particularly subclasses 300+ for digital filtering and subclasses 490+ for arithmetical processing.

716, Data Processing: Design and Analysis of Circuit or Semiconductor Mask, appropriate subclasses.

233 Branching (e.g., delayed branch, loop control, branch predict, interrupt):
This subclass is indented under subclass 220. Subject matter including means or steps for performing a change in instruction data flow brought about by instruction data execution or external stimuli.

(1) Note. This subclass provides for instruction data flow changes. Program execution flow changes for the purpose of task management and control related to process or job execution is classified elsewhere.

(2) Note. Address generation for branching is classified elsewhere.

SEE OR SEARCH CLASS:

709, Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 1+ for task management and control related to process or job execution, subclasses 3+ for process scheduling.

711, Electrical Computers and Digital Processing Systems: Memory, subclass 125 for instruction data caching, subclass 169 for memory access pipelining, and subclass 213 for address generation for branching.

714, Error Detection/Correction and Fault Detection/Recovery, appropriate subclasses, particularly subclasses 50+ for a state out of sequence error detection.

234 Conditional branching:
This subclass is indented under subclass 233. Subject matter including means or steps for supporting changes in program execution flow based upon some condition within the processor (e.g., branch if equal, branch if zero, etc.).

235 Simultaneous parallel fetching or executing of branch and fall-through path:
This subclass is indented under subclass 234. Subject matter including systems which execute in parallel both the branch taken and branch failure paths of a conditional branch until such time as the outcome of the conditional branch is known.

236 Evaluation of multiple conditions or multi-way branching:
This subclass is indented under subclass 234. Subject matter including means or steps for evaluating more than a single condition in one instruction or for choosing to branch to at least one of multiple destinations.

237 Prefetching a branch target (i.e., look ahead):
This subclass is indented under subclass 234. Subject matter including means or steps for prefetching an instruction from the target of a branch in anticipation of the branch being taken.

(1) Note. This subclass provides for prefetch in relation to a conditional branch. Generic prefetching is classified elsewhere.

(2) Note. Address generation for prefetching is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
207, for generic prefetch of instruction data.

SEE OR SEARCH CLASS:
711, Electrical Computers and Digital Processing Systems: Memory, subclass 213 for address generation for prefetching.

238 Branch target buffer:
This subclass is indented under subclass 237. Subject matter including means or steps for memorizing or holding the last several branch target addresses so that if a branch is encountered again, the target address does not have to be recalculated.

239 Branch prediction:
This subclass is indented under subclass 234. Subject matter including means or steps for attempting to theorize or guess an outcome of a branch before such outcome can be determined.

SEE OR SEARCH CLASS:
711, Electrical Computers and Digital Processing Systems: Memory, subclasses 204+ for address mapping by prediction or look-ahead.

240 History table:
This subclass is indented under subclass 239. Subject matter including means or steps for memorizing an outcome of the last several branch instructions encountered and use that to more accurately predict an outcome of that same branch instructions if they are encountered again in the future.

241 Loop execution:
This subclass is indented under subclass 233. Subject matter including means or steps for controlling an execution of a program loop.

(1) Note. This subclass provides for details of an internal control of a processor and sequencing of instruction data for a performance of loops. Programming of loops and compiling of loop statements are classified elsewhere.

(2) Note. Subroutine calling and returning is classified elsewhere.

(3) Note. Interrupt service and return is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
242, for macroinstruction routine.
243, for microinstruction subroutine.
244, for exception processing (interrupts and traps).

SEE OR SEARCH CLASS:
703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.
709, Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 1+ for task management and control related to process or job execution, and subclasses 3+ for process scheduling.
710, Electrical Computers and Digital Processing Systems: Input/Output, subclasses 260+ for interrupt service and interrupt return processing in a digital data processing system.
716, Data Processing: Design and Analysis of Circuit or Semiconductor Mask, appropriate subclasses.
717, Data Processing: Software Development, Installation, and Management, subclasses 124 through 135 for software testing or debugging and subclasses 140-161 for compilers, per se.

242 To macro-instruction routine:
This subclass is indented under subclass 233. Subject matter including means or steps for accessing and performing a particular predefined routine.

(1) Note. This subclass provides for the details of the internal sequencing and

processing of instruction data for performing routines not otherwise provided for. For example, graphic command processing, arithmetic operation command processing, and logic operation command processing are classified elsewhere.

(2) Note. The combination of an applications art area with macroinstruction or command processing is classified in the art area. For example, graphic command processing, emulators, compilers, and natural language processing are classified elsewhere.

SEE OR SEARCH CLASS:
345, Computer Graphics Processing, Operator Interface Processing, and Selective Visual Display Systems, subclass 522 for graphic command processing,
703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.
704, Data Processing: Speech Signal Processing, Linguistic, Language Translation, And Audio Compression/Decompression, subclass 9 for natural language translation.
716, Data Processing: Design and Analysis of Circuit or Semiconductor Mask, appropriate subclasses.
717, Data Processing: Software Development, Installation, and Management, subclasses 136 through 161 for compilers or translators.

243 To microinstruction subroutine:
This subclass is indented under subclass 233. Subject matter including means or steps for calling microcode subroutine from another microroutine.

(1) Note. Subroutine for industrial control or numerical control is classified elsewhere.

SEE OR SEARCH CLASS:
700, Data Processing: Generic Control Systems or Specific Applications, subclasses 1 through 89 for generic industrial or numerical controllers.

244 Exception processing (e.g., interrupts and traps):
This subclass is indented under subclass 233. Subject matter including means or steps for handling asynchronous or unexpected changes in instruction data flow.

(1) Note. This subclass provides for details of the internal operation of a processor for responding to an interrupt by the processor. Subject matter directed to queuing interrupts, prioritizing interrupts or signals in a digital data processing system is classified elsewhere.

(2) Note. Details of interrupt processing for the purposes of task management or multitasking are classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
40, for an external sync or interrupt signal in a processing architecture having sequential program control.

SEE OR SEARCH CLASS:
709, Electrical Computers and Digital Processing Systems: Multiple Computer or Process Coordinating, subclasses 8+ for task management and multitasking.
710, Electrical Computers and Digital Processing Systems: Input/Output, subclasses 260+ for interrupt queuing and prioritizing .

245 Processing sequence control (i.e., microsequencing):
This subclass is indented under subclass 220. Subject matter including means or steps for controlling a sequencing of an execution of a microinstruction.

246 Plural microsequencers (e.g., dual microsequencers):
This subclass is indented under subclass 245. Subject matter including two or more microsequencers for sequencing through microroutines.

247   Multilevel microcontroller (e.g., dual-level control store):
This subclass is indented under subclass 245. Subject matter including means or steps for sequencing microinstruction processing utilizing a multilevel (e.g., dual level) microcode (i.e., a first level microcode addresses and controls a retrieval of a second or subsequent level microcode.).

248   Writable/changeable control store architecture:
This subclass is indented under subclass 245. Subject matter having a microprogram storage that is writable/changeable so that a different microprogram may be installed.

(1)   Note. This subclass includes details of an arrangement of the micromemory within a microsequencer.

(2)   Note. Writable control store architectures are properly classified here. Also a product by process PLA operating as a microprogram ASIC could go here. However, transistor level or logic gate level chip design is classified elsewhere.

(3)   Note. Classification herein requires more than nominal recitation of microcode in combination with writable control store. Memory accessing and memory addressing are classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
37,   for a specific sequence control processing architecture with nominal recitation of EPROM.

SEE OR SEARCH CLASS:
326,   Electronic Digital Logic Circuitry, subclasses 37+ for multifunctional or programmable logic including PLA, PAL, PLD, etc.
365,   Static Information Storage and Retrieval, appropriate subclasses for details of memory design at the transistor or gate level.
703,   Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.

711,   Electrical Computers and Digital Processing Systems: Memory, subclasses 100+ for memory accessing and control.
716,   Data Processing: Design and Analysis of Circuit or Semiconductor Mask, appropriate subclasses.

300   BYTE -WORD ORDER REARRANGING, BIT -FIELD INSERTION OR EXTRACTION, STRING LENGTH DETECTING, OR SEQUENCE DETECTING:
This subclass is indented under the class definition. Subject matter having means or step for shuffling, adding, removing of bit or for recognizing a sequence of bytes in a larger string of bytes not provided for by the subclasses above.

(1)   Note. This subclass is for generic processing of digital words including sorting, list processing and bit or byte operations at the word level. Instruction processing for logical operations on digital words and digital logic, per se, is classified elsewhere.

(2)   Note. This subclass does not accept generic processing of digital words for the expressed purpose of converting one code to another code (e.g., BCD =>BINARY). These teachings are classified elsewhere. Nor does this subclass accept encryption. Encryption is classified elsewhere.

(3)   Note. Processing of digital words to an expressed filtering effect on acquired signals or an arithmetic operation on a series of digital words is classified elsewhere.

(4)   Note. Searching and sorting in databases, files, and word processing applications are not classified here and instead are classified with the respective application art areas.

SEE OR SEARCH THIS CLASS, SUBCLASS:
220+,   for specialized instruction data processing (e.g., for debugging, for logic

operations, for context preserving, etc.).

SEE OR SEARCH CLASS:
341,　Coded Data Generation or Conversion, appropriate subclasses for analog-to-digital converters and digital-to-digital code converters.
380,　Cryptography, subclasses 6+ for electrical signal masking, subclasses 9+ for electrical signal modification (e.g., scrambling).
707,　Data Processing: Database and File Management, Data Structures, or Document Processing, subclasses 1 through 206 for database and file searching and sorting.
708,　Electrical Computers: Arithmetic Processing And Calculating, subclasses 300+ for digital filtering and subclasses 490+ for arithmetical processing.

END